REMARKS

The Office Action dated July 22, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 6, 16, and 21 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-2 and 4-21 are pending in the present application and are respectfully submitted for consideration.

Claims 1-2, 4-21 Recite Patentable Subject Matter

Claims 1-2, 4-5, and 16-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takahashi et al. (JP 40927070, "Takahashi"). Applicant respectfully traverses the rejection and submits that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites an input circuit comprising, among other features, a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal, such that only a rising delay time of the node signal is shortened.

Claim 16 recites an input circuit comprising, among other features, a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to condition an amount of the current flowing through the second transistor to be increased in response to the node signal when the first MOS transistor changes its state from an activated state to a deactivated state in response to the data signal, such that only a rising delay time of the node signal is shortened

Claim 21 recites a semiconductor integrated circuit for receiving a data signal in response to rising and falling edges of a data strobe signal comprising, among other features, a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor operates to condition an amount of the current flowing through the differential circuit to be increased in response to the logic level of the differential output signal when the first transistor changes its state from an activated state to a deactivated state in response to the data strobe signal, such that a rising delay time of the logic level of the differential output signal is shortened.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicant's invention.

The Office Action characterized as allegedly disclosing "an amplifier circuit in Figures 1-5 comprising a differential circuit (N3, N4, P3, P4) a current regulating circuit (P2, N6), a constant current source (P1, N5) and a[n] even number of feedback delay elements (inverters V1, V3-V5)," and admits the Takahashi "does not disclose the limitation [of] 'the regulating circuit current increases an amount of the current flowing through the differential circuit in response to the node signal such that only rising delay time of the node signal is shortened." The Office Action further takes the position that "it would have been obvious to a person having skill in the art at the time the invention was made to select one feedback delay element for the circuit of Takahashi et al for the purpose of increase the speed cycle time of the amplifier."

Applicants submit that Takahashi fails to disclose or suggest each and every element recited in claims 1, 16 and 21 of the present application. In particular, it is submitted that Takahashi fails to disclose the current regulating circuit that conditions an amount of the current flowing through a differential circuit to be increased in response to a node signal when a first transistor changes its state form an activated state to an deactivated state in response to an external signal, such that only a rising delay time of the node signal is shortened, as recited in the claims.

For example, Takahashi fails to condition an amount of the current flowing through a differential circuit to be increased when a first transistor (P3; N3) changes its state from an activated state to a deactivated state. Specifically, in Figs. 1 and 2 of Takahashi, a transistor P2 operates to increase an amount of current after a transistor P3 is deactivated in response to a rising edge of an input signal Vin, thereby previously

boosting a voltage of a node n1 from a low level by ΔV to shorten a rising delay time of a node n1 signal when the input signal Vin falls. Furthermore, in Figs. 4 and 5 of Takahashi, a transistor N6 operates to increase an amount of current after a transistor N3 is deactivated in response to a falling edge of an input signal Vin, thereby lowering a voltage of a node n4 from a high level by ΔV.

In contrast, the current regulating circuit T_{N4} of the present invention conditions an amount of the current flowing through a differential circuit to be increased when the first transistor T_{N1} changes its state from an activated state to a deactivated state, thereby only shortening a rising delay time of the node signal. Accordingly, the present invention distinguishes over Takahashi.

Furthermore, Applicant traverses the Office Action's position that "it would have been obvious to a person having skill in the art at the time the invention was made to select one feedback delay element for the circuit of Takahashi et al for the purpose of increase the speed cycle time of the amplifier" since employing one feedback delay element is not obvious by Takahashi. Given that the transistor (P2; P6) is designed to be activated after the transistor (P3; N3) is deactivated, it is necessary to set a certain amount of delay time using some inverters (V1, V3 to V5). In other words, reducing the number of inverters shortens the delay time, and the circuit of the Takahashi may not operate in a manner as described above. In contrast, since the current regulating circuit T_{N4} already operates when the first transistor is deactivated, it is not necessary to consider such a delay time, and the current regulating circuit properly operates using an inverter the number of which is less than that of the inverters of Takahashi.

Accordingly, Applicant submits that Takahashi fails to disclose each and every element recited in claims 1, 16 and 21 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art reference must teach, i.e., identically describe, each feature of a rejected claim. As explained above, Takahashi fails to disclose or suggest each and every feature of claims 1, 16 and 21. Accordingly, Applicants respectfully submit that claims 1, 16 and 21 are not anticipated by nor rendered obvious by the disclosure of Takahashi. Therefore, Applicants respectfully submit that claims 1, 16 and 21 are allowable.

As claims 2, 4 and 5 depend from claim 1, and claims 17-20 depends from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 6-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 1 of Applicant's Admitted Prior Art ("AAPA") in view of Takahashi. Applicant respectfully traverses the rejection and submits that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 6 recites a semiconductor integrated circuit comprising, among other features, a current regulating circuit, connected to the differential circuit, which conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from

an activated state to a deactivated state in response to the external signal, such that only a rising delay time of the node signal is shortened.

Takahashi is discussed above.

AAPA is applied for allegedly teaching a circuit comprising an amplifier (2a), and a processing signal circuit or a latch circuit (3). Applicant submits that AAPA does not overcome the above-described drawback of Takahashi since it fails to disclose or suggest at least a current regulating circuit, connected to the differential circuit, which conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal, such that only a rising delay time of the node signal is shortened.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Takahashi and AAPA, taken alone or in combination, do not teach or suggest each feature recited by pending claims 6 and 16. Accordingly, for the above reasons, Applicant respectfully submits that pending claim 6 and 16 are not rendered obvious under 35 U.S.C. § 103 by the teachings of Takahashi and AAPA, and therefore, it is respectfully submitted that claims 6 and 16 are allowable.

As claims 7-15 depend from claim 6, and claims 17-20 depends from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein,

and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

Applicants respectfully request withdrawal of the rejection.

CONCLUSION

In view of the above, Applicant respectfully submits that each of claims 1-2 and 4-21 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-2 and 4-21 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108075-09014.

Respectfully submitted,

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